



Figure 1 is a schematic diagram of a semiconductor device, showing multiple stages (A1, A2, ..., An) of a signal processing circuit. Each stage includes a series of transistors (201, 202, 203, 204, 205, 206, 207) and a load resistor (208). The diagram illustrates the voltage drop (V1) and the condition  $V1 > V2$  (in case that  $V1 > 0$  and  $V2 > 0$ ) across the stages.



FIG. 3A

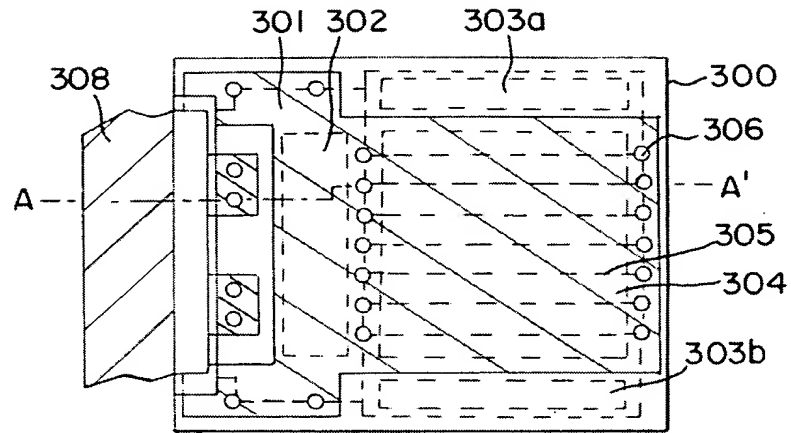


FIG. 3B

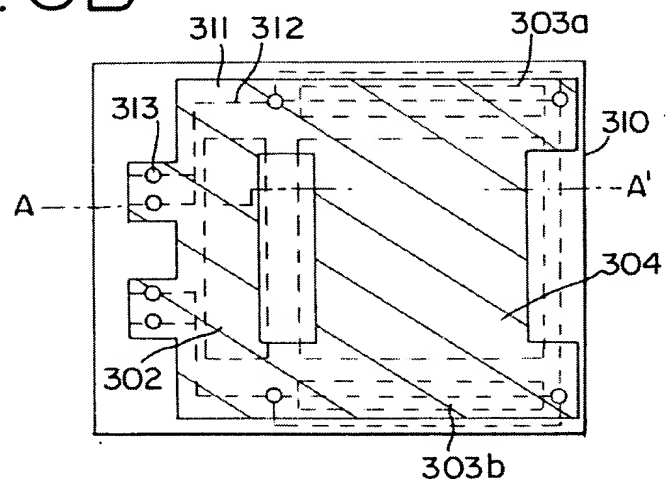


FIG. 3C

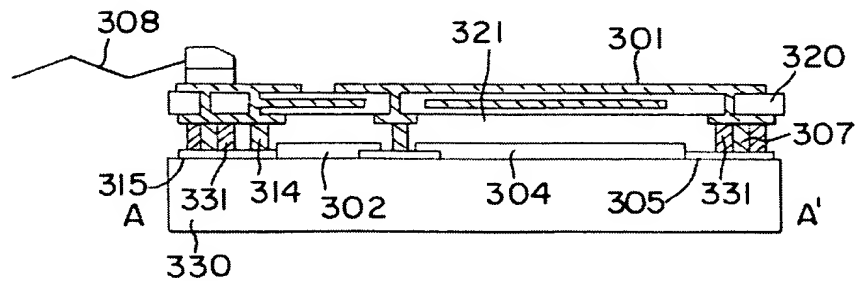




FIG. 4A

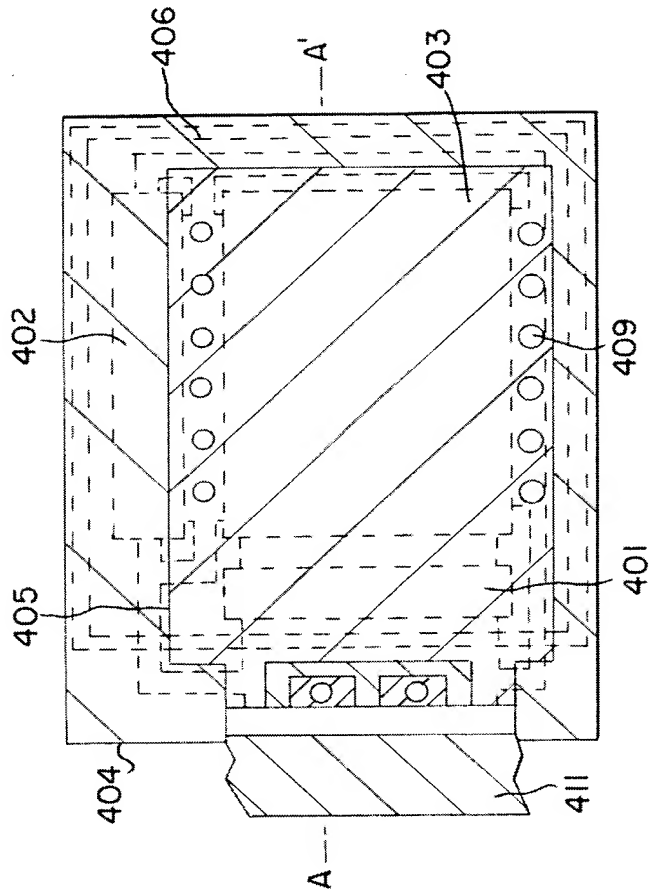


FIG. 4B

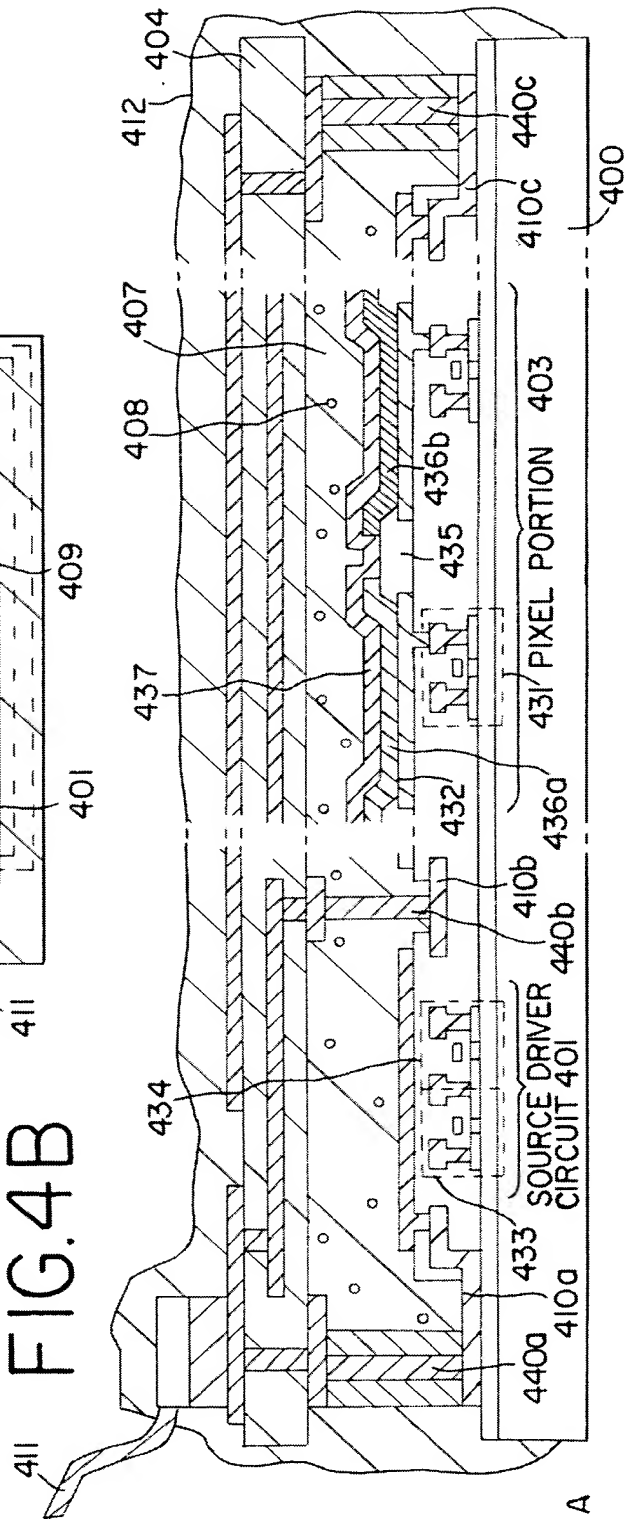




FIG. 5A

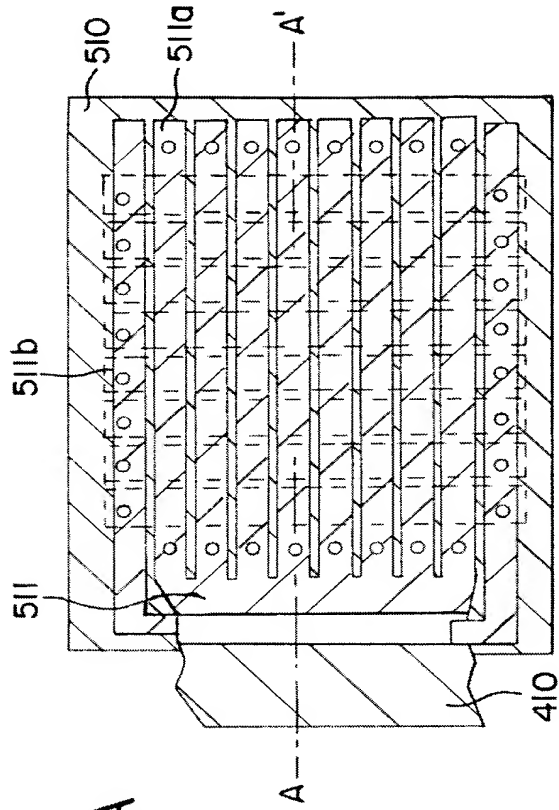


FIG. 5B

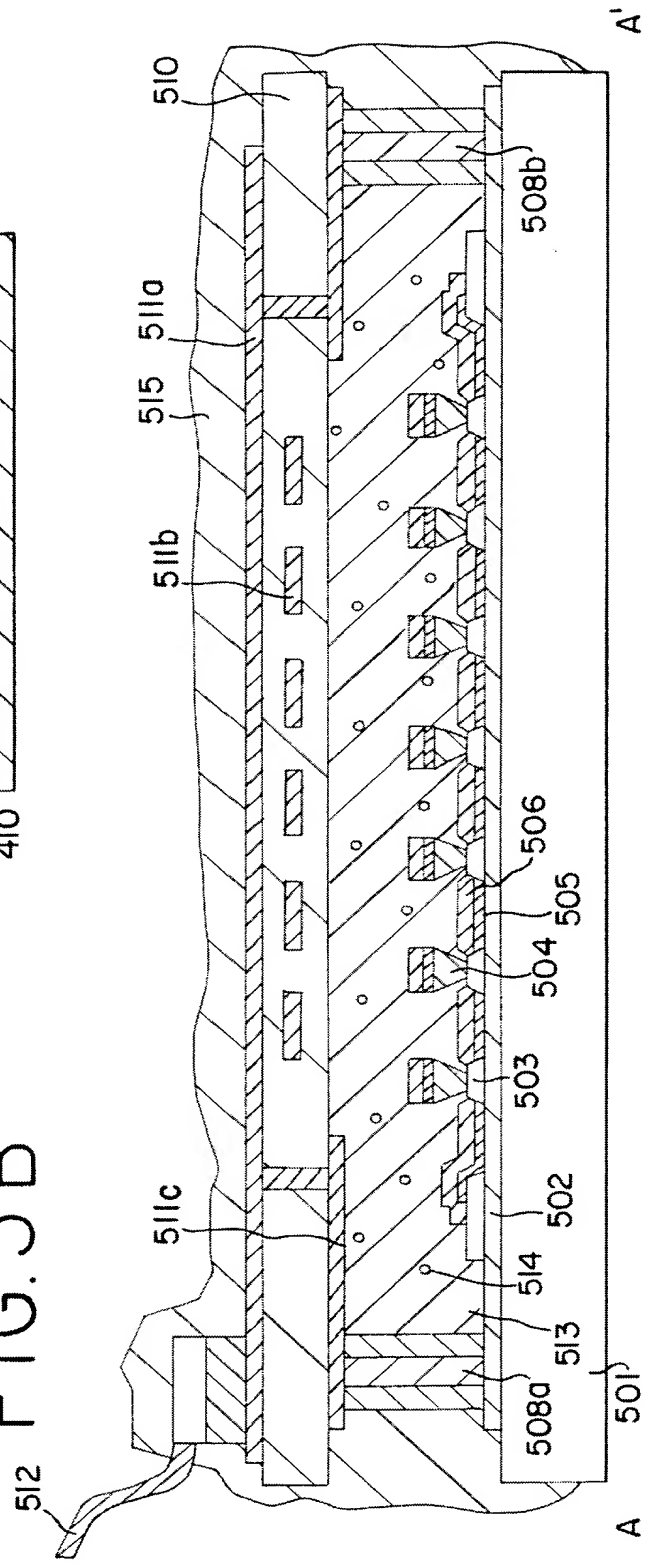




FIG. 6

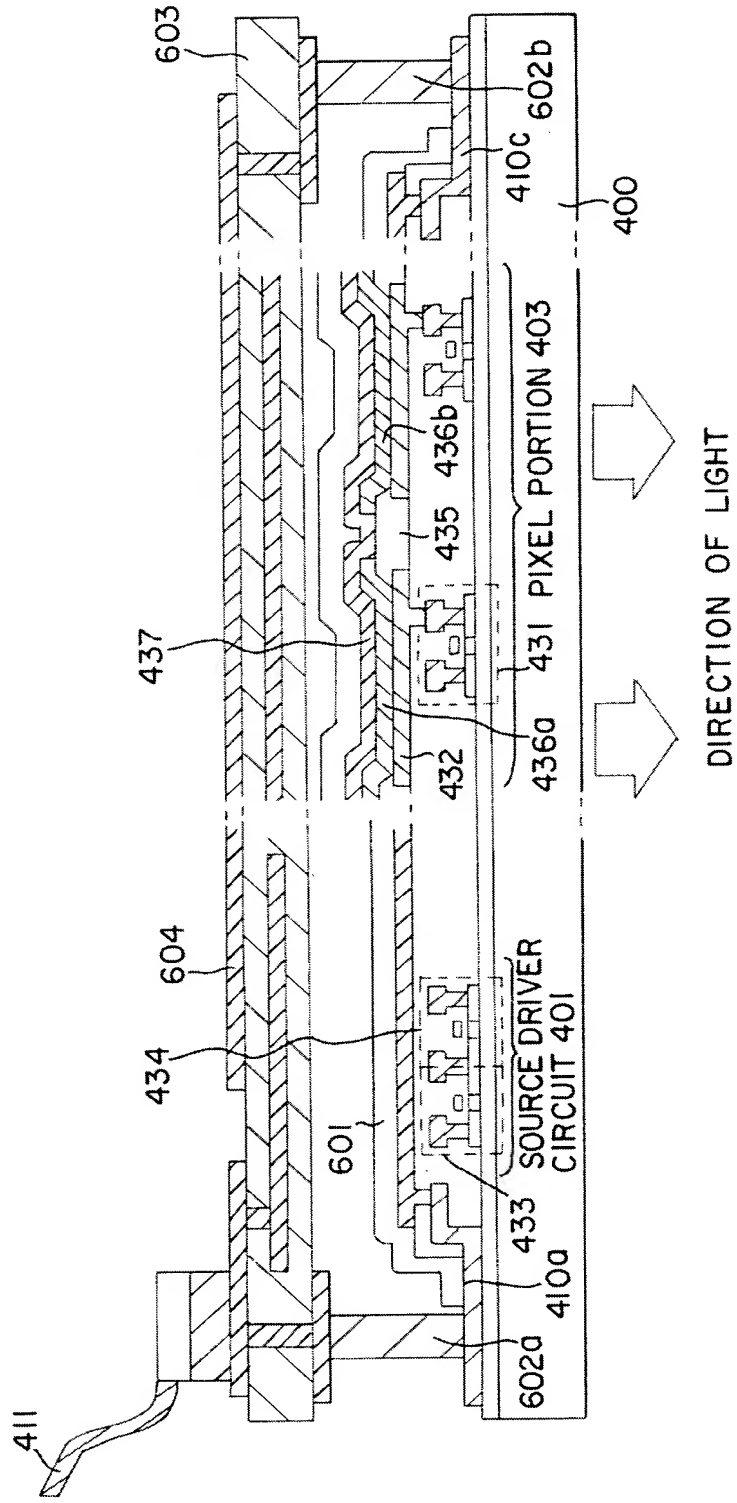




FIG. 7

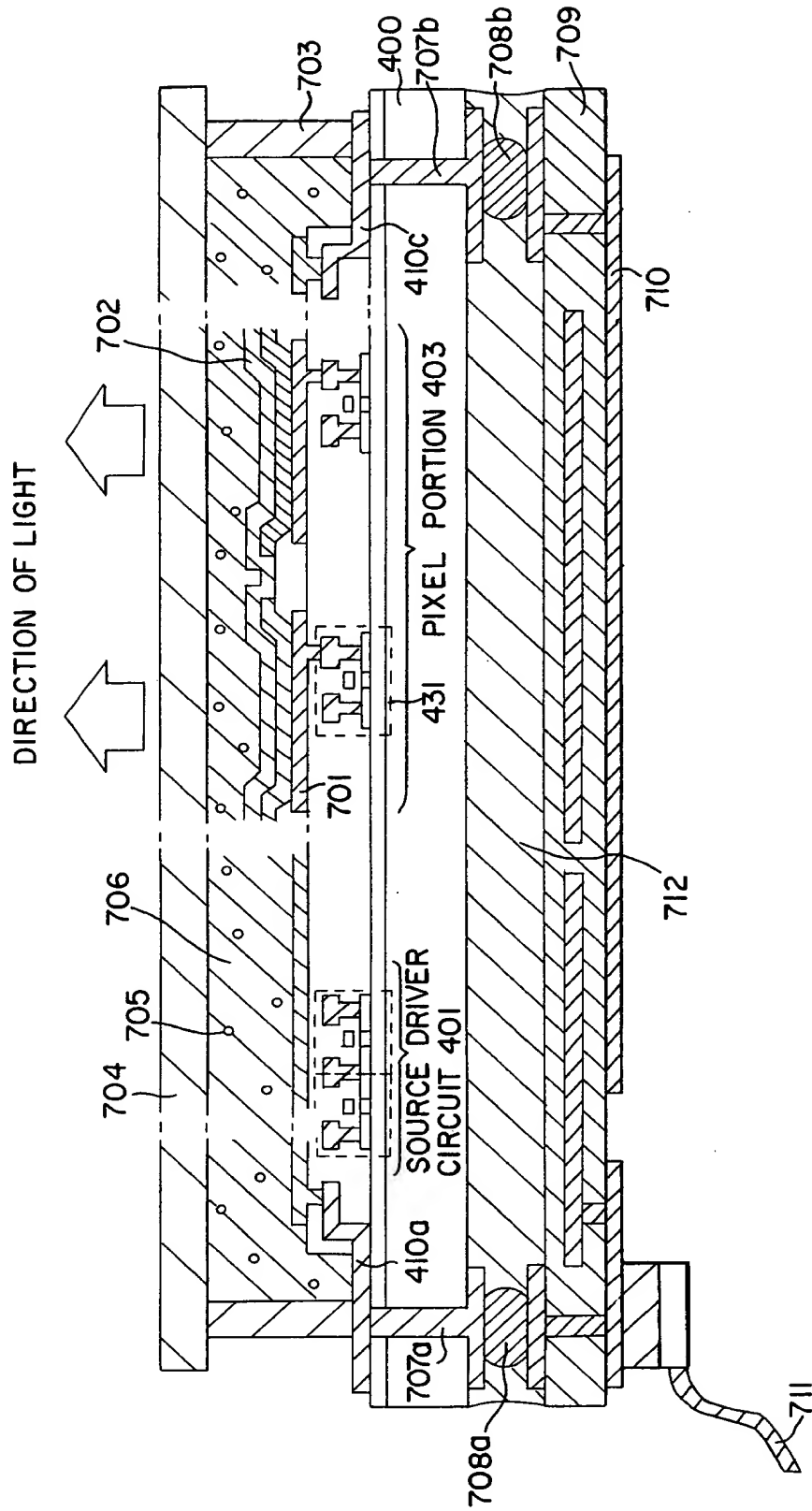




FIG. 8A

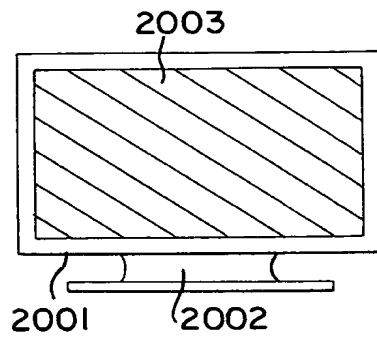


FIG. 8B

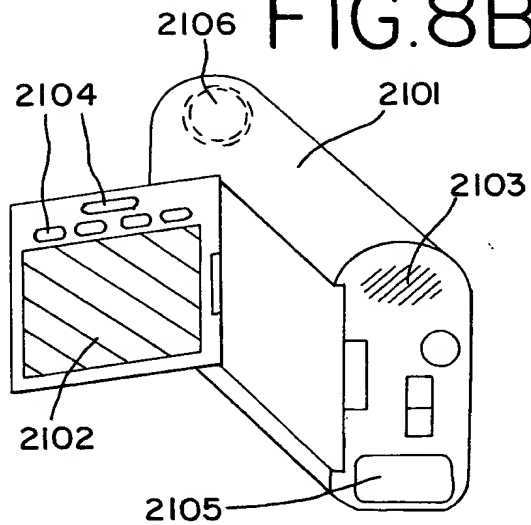


FIG. 8C

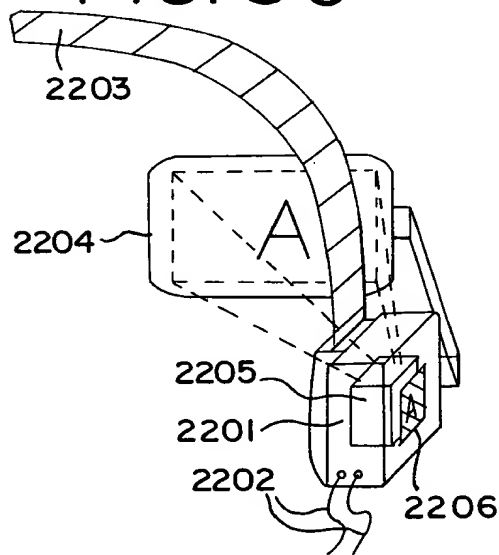


FIG. 8D

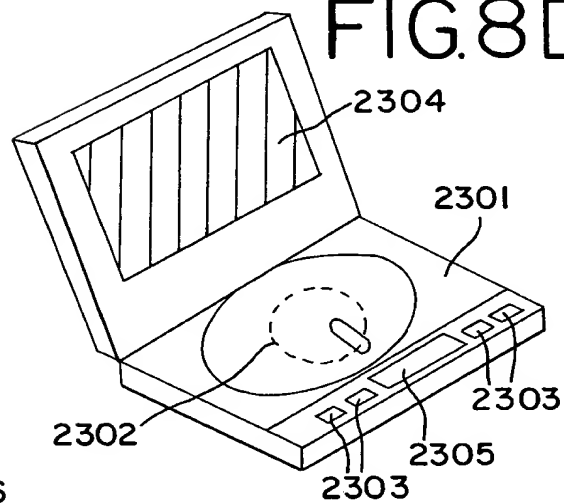


FIG. 8E

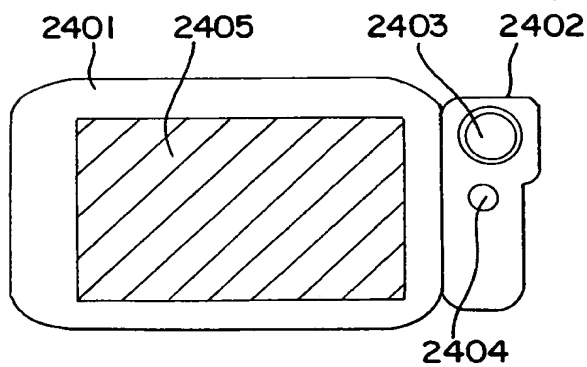


FIG. 8F

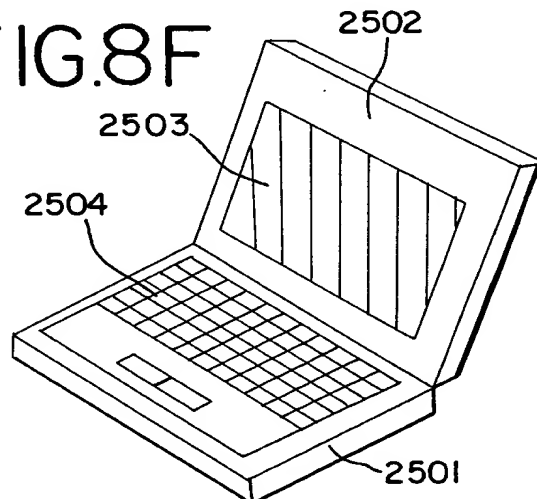




FIG. 9A

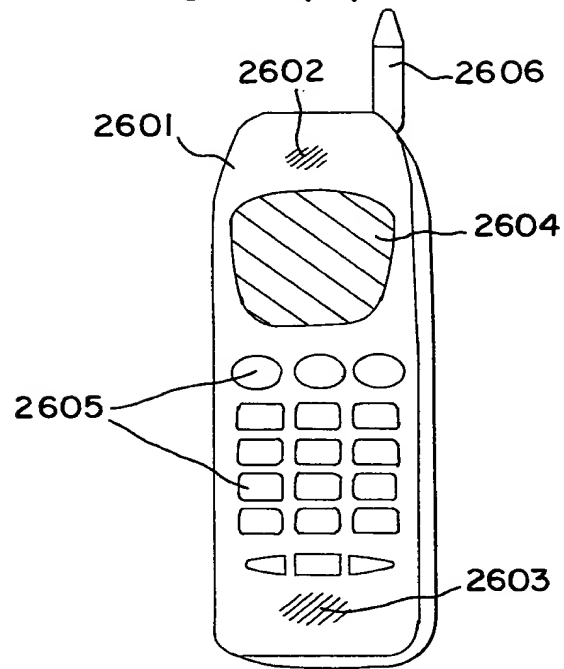


FIG. 9B

